



**Embedded Panel Controller
- EPC25 CPU Module -
Hardware Manual**

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Revision History

Date	Doc. Rev.	Description	Autor
25.11.2014	1.0	Initial Release	PJ/VH

Table 1: Revision History

Module Concept

The EPC25 System on Chip (SoC) Module is a cost-efficient and high reliable CPU module based on Texas Instruments TM4V129X Cortex-M SoC. The many capabilities in numerous areas of industrial control technology make the EPC25 to an outstanding CPU module.

The EPC25 impresses with a multiplicity of possible interfaces like 1x Ethernet with integrated PHY with IEEE 1588 PTP hardware support, 8x UART, 4x SSI, 10 x I²C, 2x CAN 2.0 A/B, 1x USB 2.0 OTG/Host/Device with ULPI interface option and Link Power Management (LPM) support, LCD & TFT Controller (up to 24 bits per pixel), ADC Inputs, PWM Quadrature Encoder, microSD, SDRAM and many GPIOs. Further the multiplexing of GPIOs makes it possible to change functionality of signals on the same package pins.

The module uses Q7 MXM 230 pin as mating connector and has smaller form factor than standard Q7 module. The module impresses with its compact size of only 40 mm x 70 mm.

Module Block Diagram

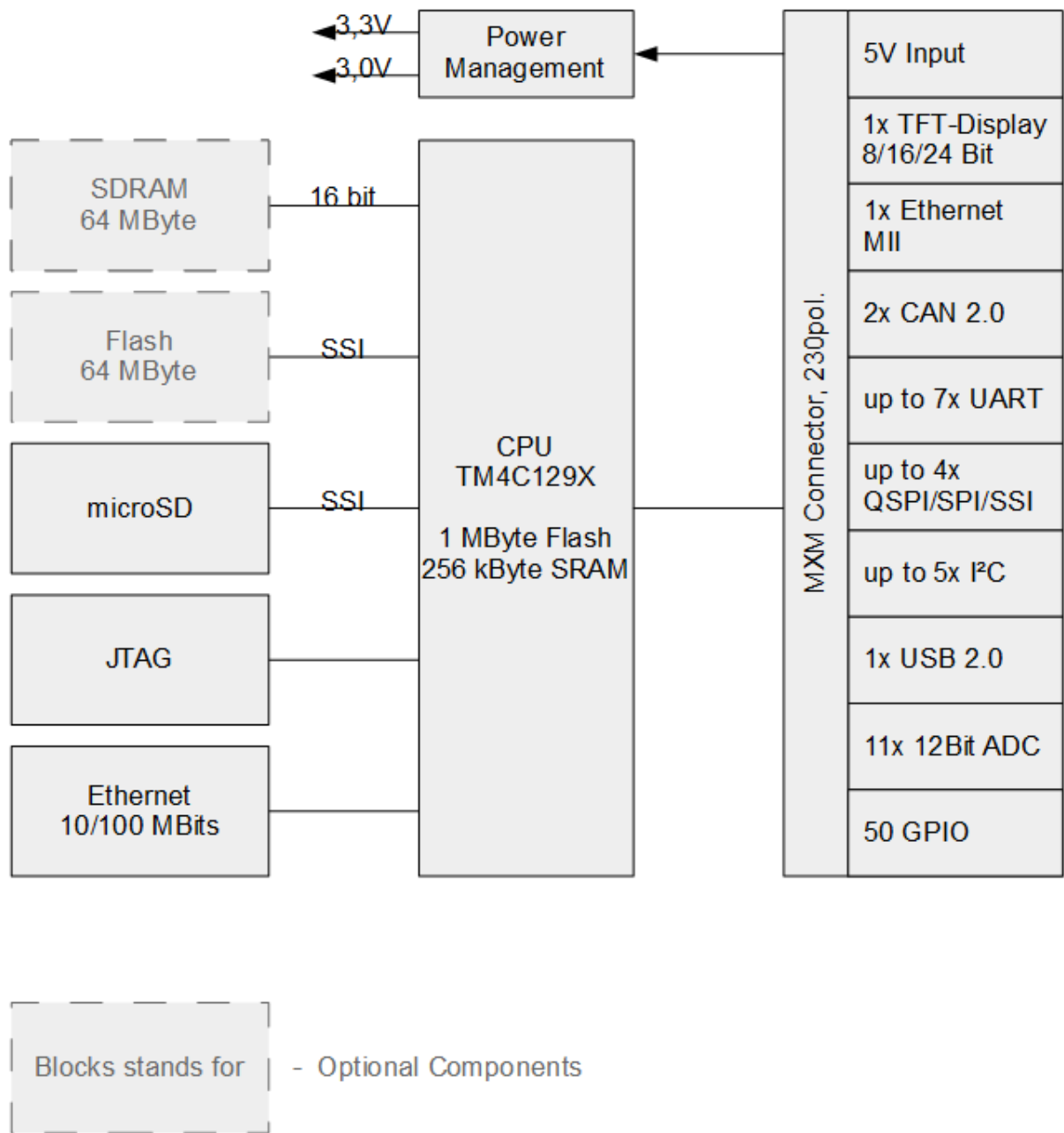


Figure 1: Block Diagram

Overview

Top

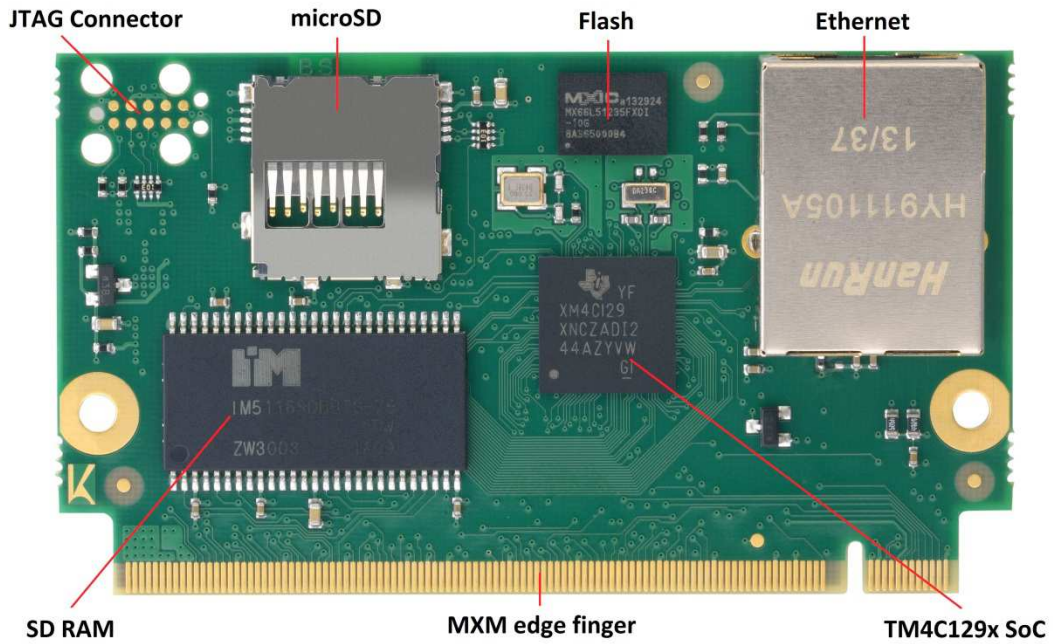


Figure 2: Overview Top

Component Placement

Top View

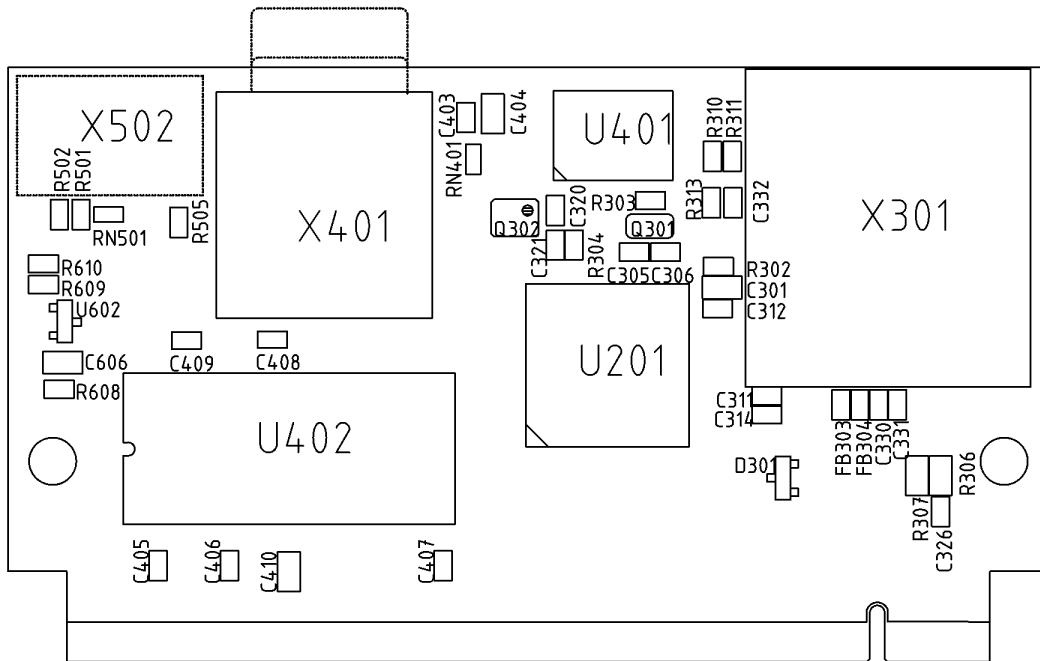


Figure 3: Component Placement - Top View

Bottom View

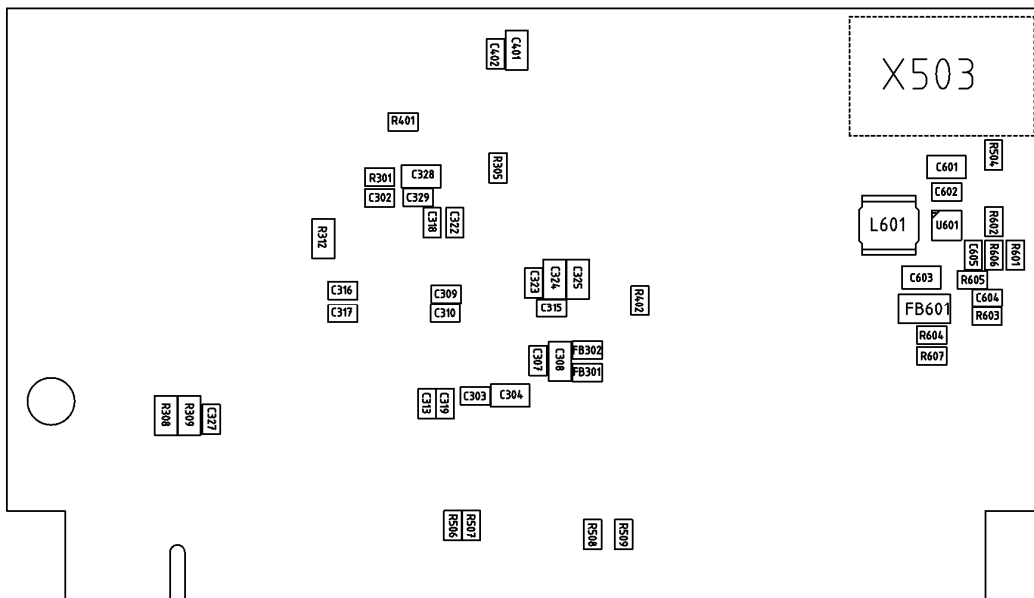


Figure 4: Component Placement - Bottom View

Power Supply

Primary System Power

The EPC25 operates off of a primary voltage supply with a nominal value of $+5.0\text{ V} \pm 5\%$.

On-board switching regulators generate the 3.3 V voltage supply and the 3.0V reference voltage required by the TM4C129X processor and on-board components from the primary 5.0 V supplied to the SOM.

For proper operation the EPC25 must be supplied with a voltage source of 5.0 V with at least 1.0 A capacity at the VCC pins on the EPC25 - Connector.

TM4C129X SoC

Description CPU

Tiva™ C Series microcontrollers integrate a large variety of rich communication features to enable a new class of highly connected designs with the ability to allow critical, real-time control between performance and power. The microcontrollers feature integrated communication peripherals along with other high-performance analog and digital functions to offer a strong foundation for many different target uses, spanning from human machine interface to networked system management controllers [1].

Features

- Performance
 - ARM® Cortex™-M4F processor core
 - 120-MHz operation; 150 DMIPS performance
 - 1024 KB Flash memory
 - 256 KB single-cycle System SRAM
 - 6KB of EEPROM
 - Internal ROM loaded with TivaWare™ for C Series software
 - 8-/16-/32-bit dedicated External Peripheral Interface (EPI) for peripherals and memory
- Security
 - Cyclical Redundancy Check (CRC) hardware with 16-/32-bit Hash function that supports four CRC forms
 - Advanced Encryption Standard (AES) hardware-accelerated data encryption and decryption based on 128-, 192-, and 256-bit keys
 - Data Encryption Standard (DES) block cipher implementation with 168-bit effective key length
 - Hardware Accelerated Hash (SHA/MD5) advanced hash engine that supports SHA-1, SHA-2 or MD5 Hash computation
 - Support for four tamper inputs and configurable tamper event response
- Communication Interfaces
 - Eight Universal Asynchronous Receivers/Transmitters (UARTs)
 - Four Quad Synchronous Serial Interface (QSSI) modules with Bi-, Quad- and advanced SSI support
 - Ten Inter-Integrated Circuit (I²C) modules with four transmission speeds including high-speed mode
 - Two Controller Area Network (CAN) 2.0 A/B controllers
 - 10/100 Ethernet MAC
 - Ethernet PHY with IEEE 1588 PTP hardware support
 - Universal Serial Bus (USB) 2.0 OTG/Host/Device with ULPI interface option and Link Power Management (LPM) support
- System Integration
 - ARM® PrimeCell® 32-channel configurable Micro Direct Memory Access (μDMA) controller
 - Configurable LCD controller with passive and active matrix LCD panel support
 - Eight 16/32-bit General-Purpose Timer (GPTM) blocks
 - Two watchdog timers
 - Low-power battery-backed Hibernation module
 - 18 physical General-Purpose Input/Output (GPIO) blocks
- Advanced Motion Control
 - One Pulse Width Modulator (PWM) module, with four PWM generator blocks and a control block, for a total of 8 PWM outputs
 - One Quadrature Encoder Interface (QEI) module
- Analog Support
 - Two 12-bit Analog-to-Digital Converter (ADC) modules, each with a maximum sample rate of one million samples/second
 - Three independent integrated analog comparators
 - 16 digital comparators
- System Management
 - 1-Wire module
- One JTAG module with integrated ARM Serial Wire Debug (SWD)
- 212-ball BGA package
- Operating Range (Ambient)
 - Industrial (-40°C to 85°C) temperature range
 - Extended (-40°C to 105°C) temperature range [2]

Parameters

	TM4C129XNCZAD
Pin & Package	212 NFBGA
CPU	ARM Cortex-M4
Flash (KB)	1024
SRAM (kB)	256
Max Speed (MHz)	120
Motion PWM Outputs	8
QEI	1
GPIOs	140
USB D, H/D, or OTG	OTG
SSI/SPI	4
I2C	10
UART	8
ADC Channels	24
ADC Resolution (Bits)	12
CAN MAC	2
SysTick	Yes
Operating Temperature Range (°C)	-40 to 85 -40 to 105
External Peripheral Interface	Yes
10/100 Ethernet MAC+PHY	Yes
USB High-Speed with ULPI	Yes
10/100 Ethernet MAC	Yes
LCD Controller	Yes
Data Protection	Yes
1-Wire Master	1
Bi- and Quad- SSI/SPI	Yes

Table 2: TM4C129X Parameters [3]

Functional Block Diagram

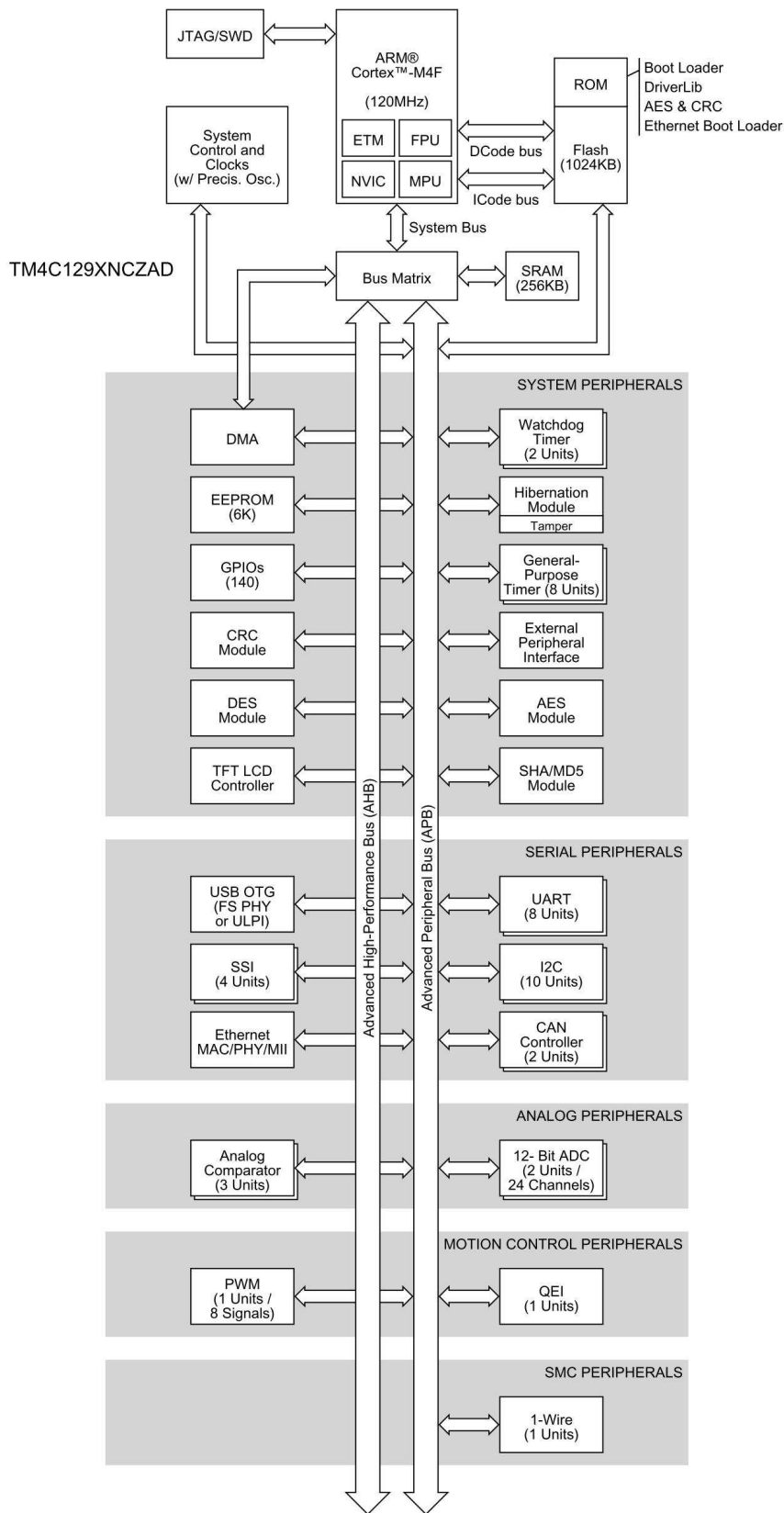


Figure 5: TM4C129X Block Diagram [4]

Mechanical Dimension

Drawing

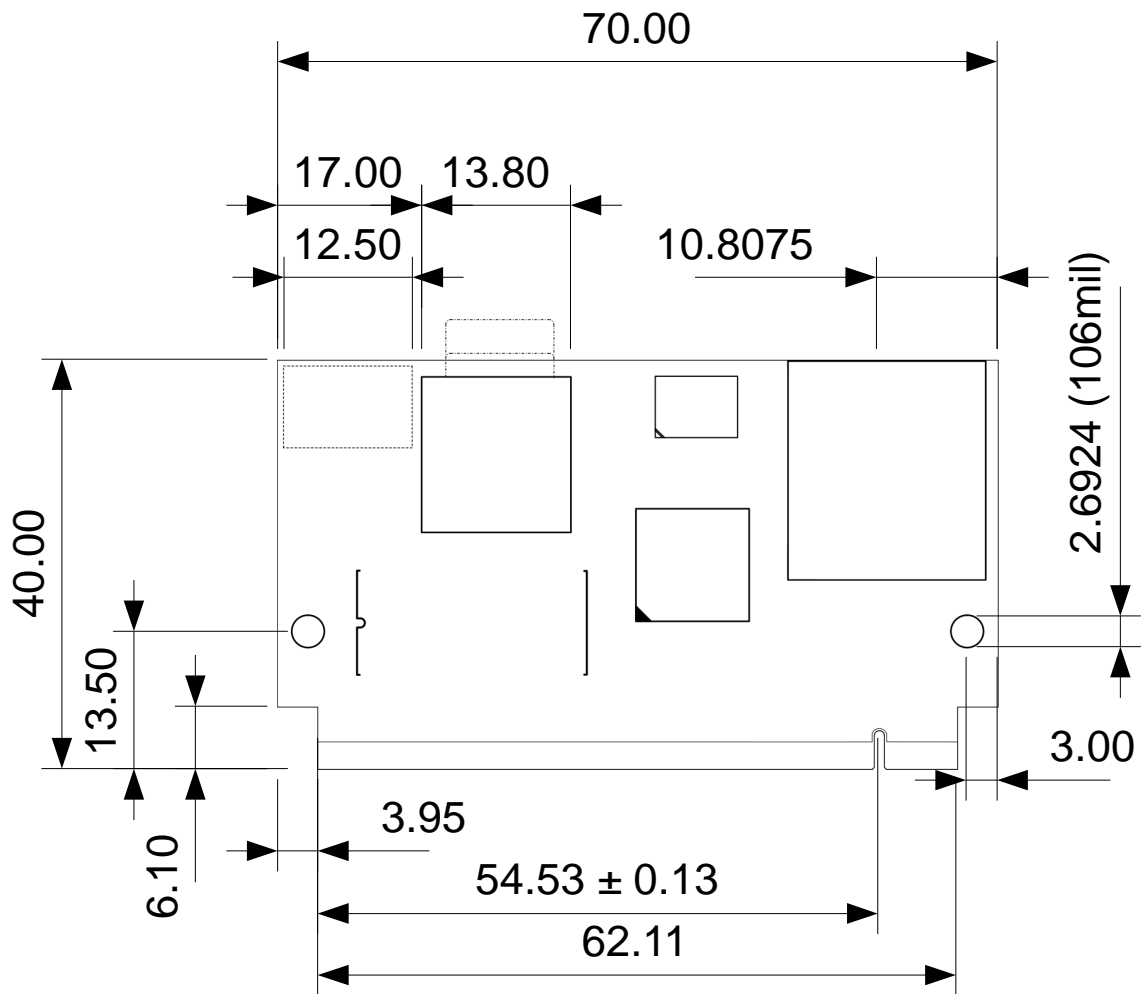


Figure 6: Mechanical Dimension - Drawing

Dimension/Weight

Dimensions	40 mm x 70 mm
Board	1,2 mm
Component height top	1,2 mm without RJ45 13,5 mm with RJ45
Component height bottom	2,5
Weight	~ 15 g

Table 3: Mechanical Dimension - Dimension/Weight

Interface

Module plug connectors

MXM Connector
0,5 mm Pitch, 230 pol.



Figure 7: MXM Connector

Manufacturer	Order number
Foxconn	ASOB32*-S78Q-7H
YAMAICHI	BEC-0.5-230-S9-BFR-EDC
Aces Electronic Co., Ltd.	88882-2D0*

Table 4: List of manufacturers

Connector - Pin assignment

Pin	I/O	Recommended configuration 1	Recommended configuration 2	Recommended configuration 3
1	GND			
2	GND			
3	PE3	AIN0		
4	PE2	AIN1		
5	PE1	AIN2		
6	PE0	AIN3		
7	PD1	AIN14	I2C7SDA	C1o
8	PD0	AIN15	I2C7SCL	C0o
9	PK2	AIN18		
10	PK3	AIN19		
11	PE6	AIN20		
12	PH5			
13	PE7	AIN21		
14	nHIB			
15	nWAKE			
16	VBAT			
17	nRESET*			
18	EN0TXOP			
19	ENORXIP			
20	EN0TXON			
21	ENORXIN			
22	+3.3V*			
23	GND			
24	GND			
25	GND			
26	PP7	AIN22	AIN22	
27	N. C.			
28	N. C.			
29	N. C.			
30	N. C.			
31	N. C.			
32	N. C.			
33	N. C.			
34	GND			
35	PP6	AIN23	AIN22	
36	N. C.			
37	N. C.			
38	N. C.			
39	GND			

Pin	I/O	Recommended configuration 1	Recommended configuration 2	Recommended configuration 3
40	GND			
41	N. C.			
42	N. C.			
43	N. C.			
44	N. C.			
45	N. C.			
46	N. C.			
47	N. C.			
48	N. C.			
49	N. C.			
50	N. C.			
51	N. C.			
52	N. C.			
53	N. C.			
54	N. C.			
55	N. C.			
56	N. C.			
57	GND			
58	GND			
59	N. C.			
60	PB4	SSI1Fss	AIN10	I2C5SCL
61	PE5	SSI1XDAT1	AIN8	
62	PE4	SSI1XDAT0	AIN9	
63	PB5	SSI1Clk	AIN11	I2C5SDA
64	N. C.			
65	PA3	SSIOFss	T1CCP1	
66	PA5	SSIOXDAT1	T2CCP1	
67	PA4	SSIOXDAT0	T2CCP0	
68	PA2	SSIOClk	T1CCP0	
69	PD3	I2C8SDA	AIN12	
70	PD2	I2C8SCL	AIN13	C2o
71	PB7	I2C6SDA		T6CCP1
72	PB6	I2C6SCL		T6CCP0
73	GND			
74	GND			
75	PP0	U6Rx	T6CCP0	C2+
76	PP1	U6Tx	T6CCP1	C2-
77	PH6	U5Rx		
78	PH7	U5Tx		
79	PK0	U4Rx	AIN16	
80	PK1	U4Tx	AIN17	

Pin	I/O	Recommended configuration 1	Recommended configuration 2	Recommended configuration 3
81	PD4	U2Rx	AIN7	T3CCP0
82	PD5	U2Tx	AIN6	T3CCP1
83	PQ4	U1Rx		
84	PQ5	U1Tx		
85	PN0	U1RTS		
86	PN1	U1CTS		
87	PJ0	U3Rx		
88	PJ1	U3Tx		
89	PP4	U3RTS		
90	PP5	U3CTS		
91	N. C.			
92	N. C.			
93	PA1	CAN0Tx		
94	PA0	CAN0Rx		
95	N. C.			
96	N. C.			
97	GND			
98	GND			
99	PF5	SSI3XDAT3		
100	PF4	SSI3XDAT2	ENOLED1	M0FAULT0
101	PF0	SSI3XDAT1	ENOLED0	M0PWM0
102	PF1	SSI3XDAT0	ENOLED2	M0PWM1
103	PF3	SSI3Clk		M0PWM3
104	PF2	SSI3Fss		M0PWM2
105	PQ7	U1RI		
106	PQ6	U1DTR		
107	PN2	U1DCD		
108	PN3	U1DSR		
109	N. C.			
110	N. C.			
111	PM7	TMPR0	T5CCP1	
112	PM6	TMPR1	T5CCP0	
113	PM5	TMPR2	T4CCP1	
114	PM4	TMPR3	T4CCP0	
115	PD7	NMI	AIN4	
116	PQ0	EPIOS20	EPIOS20	
117	GND			
118	GND			
119	PQ1	EPIOS21	EPIOS21	
120	PQ2	EPIOS22	EPIOS22	
121	PQ3	EPIOS23	EPIOS23	

Pin	I/O	Recommended configuration 1	Recommended configuration 2	Recommended configuration 3
122	PK7	EPIOS24	EPIOS24	
123	N. C.			
124	N. C.			
125	PD6	USBOEPEN	USBOEPEN	USBOEPEN
126	N. C.			
127	N. C.			
128	N. C.			
129	PB0	USB0ID	USB0ID	USB0ID
130	N. C.			
131	PL7	USB0DM	USB0DM	USB0DM
132	N. C.			
133	PL6	USB0DP	USB0DP	USB0DP
134	N. C.			
135	GND			
136	GND			
137	PB1	USBOVBUS	USBOVBUS	USBOVBUS
138	N. C.			
139	PA6	EPIOS8	EPIOS8	
140	PA7	EPIOS9	EPIOS9	
141	GND			
142	GND			
143	PG1	EPIOS10	EPIOS10	
144	PG0	EPIOS11	EPIOS11	
145	PM3	EPIOS12	EPIOS12	
146	PM2	EPIOS13	EPIOS13	
147	GND			
148	GND			
149	PM1	EPIOS14	EPIOS14	
150	PM0	EPIOS15	EPIOS15	
151	PL0	EPIOS16	EPIOS16	
152	PL1	EPIOS17	EPIOS17	
153	PL2	EPIOS18	EPIOS18	
154	PL3	EPIOS19	EPIOS19	
155	PK4	EPIOS32	EPIOS32	
156	PK5	EPIOS31	EPIOS31	
157	PL4	EPIOS26	EPIOS26	
158	PP3	EPIOS30	EPIOS30	
159	GND			
160	GND			
161	PB3	EPIOS28	EPIOS28	
162	PP2	EPIOS29	EPIOS29	

Pin	I/O	Recommended configuration 1	Recommended configuration 2	Recommended configuration 3
163	PK6	EPIOS25	EPIOS25	
164	PH0	EPIOS0	EPIOS0	
165	GND			
166	GND			
167	PH1	EPIOS1	EPIOS1	
168	PH2	EPIOS2	EPIOS2	
169	PH3	EPIOS3	EPIOS3	
170	PC7	EPIOS4	EPIOS4	C0-
171	PC6	EPIOS5	EPIOS5	C0+
172	PC5	EPIOS6	EPIOS6	C1+
173	PC4	EPIOS7	EPIOS7	C1-
174	PN5	EPIOS35	EPIOS35	
175	PB2	EPIOS27	EPIOS27	
176	PN4	EPIOS34	EPIOS34	
177	PL5	EPIOS33	EPIOS33	
178	PF6	LCDMCLK		
179	PS3	LCDDATA23	M0FAULT3	
180	PS2	LCDDATA22	M0FAULT2	
181	PS1	LCDDATA21	M0FAULT1	
182	PS0	LCDDATA20	M0FAULT0	
183	GND			
184	GND			
185	PT3	LCDDATA19		
186	PT2	LCDDATA18		
187	PJ5	LCDDATA17		
188	PJ4	LCDDATA16		
189	PR1	LCDFP	M0PWM1	
190	PR2	LCDLP	M0PWM2	
191	PR0	LCDCP	M0PWM0	
192	PJ6	LCDAC		
193	PR4	LCDDATA00	M0PWM4	
194	PR5	LCDDATA01	M0PWM5	
195	PF7	LCDDATA02		
196	PR3	LCDDATA03	M0PWM3	
197	GND			
198	GND			
199	PR6	LCDDATA04	M0PWM6	
200	PR7	LCDDATA05	M0PWM7	
201	PS4	LCDDATA06	PhA0	
202	PS5	LCDDATA07	PhB0	
203	PS6	LCDDATA08	IDX0	

Pin	I/O	Recommended configuration 1	Recommended configuration 2	Recommended configuration 3
204	PS7	LCDDATA09		
205	PT0	LCDDATA10		
206	PT1	LCDDATA11		
207	PN7	LCDDATA12		
208	PN6	LCDDATA13		
209	PJ2	LCDDATA14		
210	PJ3	LCDDATA15		
211	GND			
212	GND			
213	GND			
214	GND			
215	N. C.			
216	N. C.			
217	+5V			
218	+5V			
219	+5V			
220	+5V			
221	+5V			
222	+5V			
223	+5V			
224	+5V			
225	+5V			
226	+5V			
227	+5V			
228	+5V			
229	+5V			
230	+5V			

Table 5: Connector - Pin assignment

For detailed information about GPIO Pins and I/O Functions see chapter:
31.4 GPIO Pins and Alternate Functions [4]

Description of Signals *)

Pin	Name	Description
17	nRESET	Power Good Output from 3.3V Voltage Regulator
22	+3.3V	+3.3V Output with max. 20mA

Used Signals for SDRAM

Used Signals for SDRAM from External Peripheral Interface.

If SDRAM is stuffed the signals below are used, they have to be not connected on the baseboard, because collisions can happen.

If SDRAM is not stuffed the signals below can be free used for other customer purpose.

Pin	Signal/IO_Function	Description
164	EPIOS0	Address/Data 0
167	EPIOS1	Address/Data 1
168	EPIOS2	Address/Data 2
169	EPIOS3	Address/Data 3
170	EPIOS4	Address/Data 4
171	EPIOS5	Address/Data 5
172	EPIOS6	Address/Data 6
173	EPIOS7	Address/Data 7
139	EPIOS8	Address/Data 8
140	EPIOS9	Address/Data 9
143	EPIOS10	Address/Data 10
144	EPIOS11	Address/Data 11
145	EPIOS12	Address/Data 12
146	EPIOS13	BA 0/Data 13
149	EPIOS14	BA 1/Data 14
150	EPIOS15	Data 15
151	EPIOS16	DQML
152	EPIOS17	DQMH
153	EPIOS18	CASn
154	EPIOS19	RASn
161	EPIOS28	WEn
162	EPIOS29	CSn
158	EPIOS30	CKE
156	EPIOS31	CLK

Table 6: Used Signals for SDRAM

Used Signals for Flash and micro SD

Used Signals for Flash.

Pin	Signal/IO_Function	Description	PULLUP/ PULLDOWN _VALUE
-	nRESET	Reset [low active]	PU_10k
-	PG5_SSI2DAT0	Data 0	
-	PG4_SSI2DAT1	Data 1	
-	PG3_SSI2DAT2	Data 2	
-	PG2_SSI2DAT3	Data 3	
-	PG6_SSI2FSS	CSn	PU_10k
-	PG7_SSI2CLK	CLK	

Table 7: Used Signals for Flash

Used Signals for micro SD.

Pin	Signal/IO_Function	Description	PULLUP/ PULLDOWN _VALUE
-	PG5_SSI2DAT0	Data 1	
-	PG4_SSI2DAT1	Data 2	
-	PH4	Chip Select	PU_10k
-	PG7_SSI2CLK	CLK	
-	PJ7	Card Detect	PU_10k

Table 8: Used Signals for micro SD

Product Features and Specifications

Product Key – Ordering Information

See Price and Ordering Information (POI) sheet.

Function Description: Interfaces

JTAG

JTAG (Joint Test Action Group) is the common name for IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture.

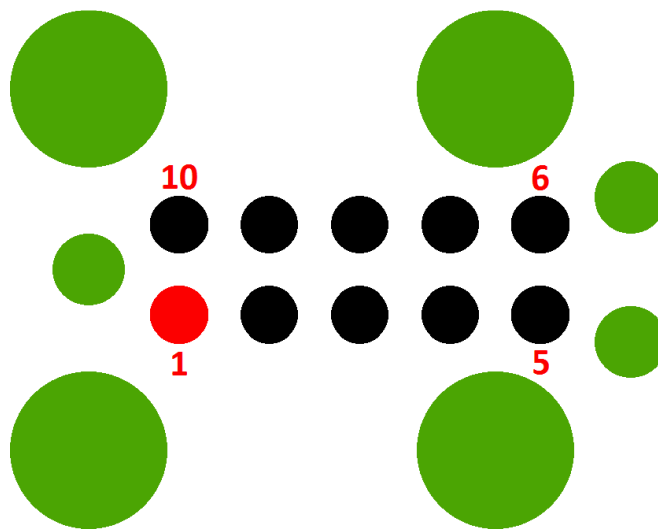


Figure 8: JTAG Connector

JTAG	Direction	Signal	PULLUP/ PULLDOWN _VALUE
1	O	nRESET	PU_10k
2	O	JTAG_TDI	PU_10k
3	I	JTAG_TDO	PU_10k
4	O	JTAG_TMS	PU_10k
5	O	JTAG_TCK	PD_10k
6	O	nRESET	PU_10k
7		DGND	
8		DGND	
9		DGND	
10		+3.3V	

Table 9: JTAG Connector

Manufacturer	Order number
Tag-Connect	TC2050-IDC

Table 10: Tag-Connect

List of References

- [1] Texas Instruments Incorporated, "TM4C129XNCZAD - Description," [Online]. Available: <http://www.ti.com/product/TM4C129XNCZAD/description#descriptions>. [Accessed 28 10 2014].
- [2] Texas Instruments Incorporated, "TM4C129XNCZAD - Features," [Online]. Available: <http://www.ti.com/product/TM4C129XNCZAD/description#features>. [Accessed 28 10 2014].
- [3] Texas Instruments Incorporated, "TM4C129XNCZAD - Parametrics," [Online]. Available: <http://www.ti.com/product/TM4C129XNCZAD/description#parametrics>. [Accessed 28 10 2014].
- [4] Texas Instruments Incorporated, "Tiva C Series TM4C129XNCZAD MicrocontrollerData Sheet (Rev. B)," [Online]. Available: <http://www.ti.com/lit/ds/symlink/tm4c129xnczad.pdf>. [Accessed 28 10 2014].