

**Embedded Panel Controller
- EPC 35 CPU Module -
Hardware Manual**

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Revision History

Date	Doc. Rev.	Description	Author
10.01.2014	1.0	Initial release	RB/VH
24.11.2014	1.1	Review	PJ/VH

Table 1: Revision History

Module Concept

The EPC35 SoC Module is a cost-efficient and high reliable CPU module based on Texas Instruments AM335x Cortex-A8 Soc. The many capabilities in numerous areas of industrial control technology make the EPC35 to an outstanding CPU module.

The EPC35 impresses with a multiplicity of possible interfaces like 2 x Gigabit Ethernet, 2 x High-Speed USB, 6 x UART, 2 x SPI, 3 x SDIO, 3 x I²C, 2 x CAN 2.0B, 8 ADC Inputs, PWM, Quadrature Encoder and many GPIOs. Further the multiplexing of GPIO's makes it possible to change functionality of signals on the same package pins.

The hardware support of industrial control interfaces like EtherCAT, PROFIBUS, PROFINET and Sercos is possible through special Programmable Realtime Units (PRU).

The module uses Q7 MXM 230 pin as mating connector and has smaller form factor than standard Q7 module. The standardized pin out for Q7 standard connector cannot be used because of lack of non-standardized signal for ARM architecture within Q7 standard. The module impresses with its compact size of only 40 mm x 70 mm.

Module Block Diagram

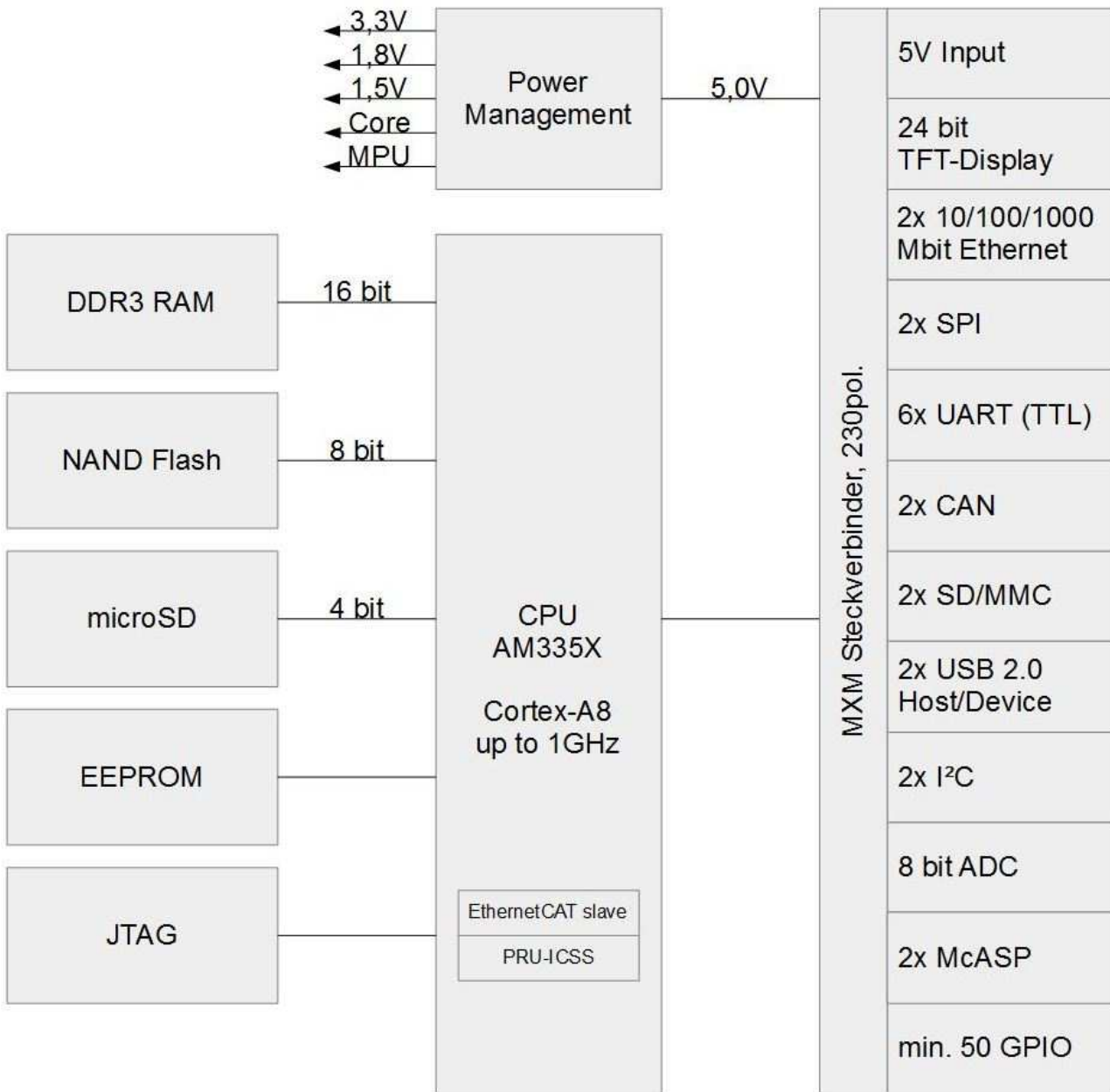


Figure 1: Block Diagram

Overview

Top

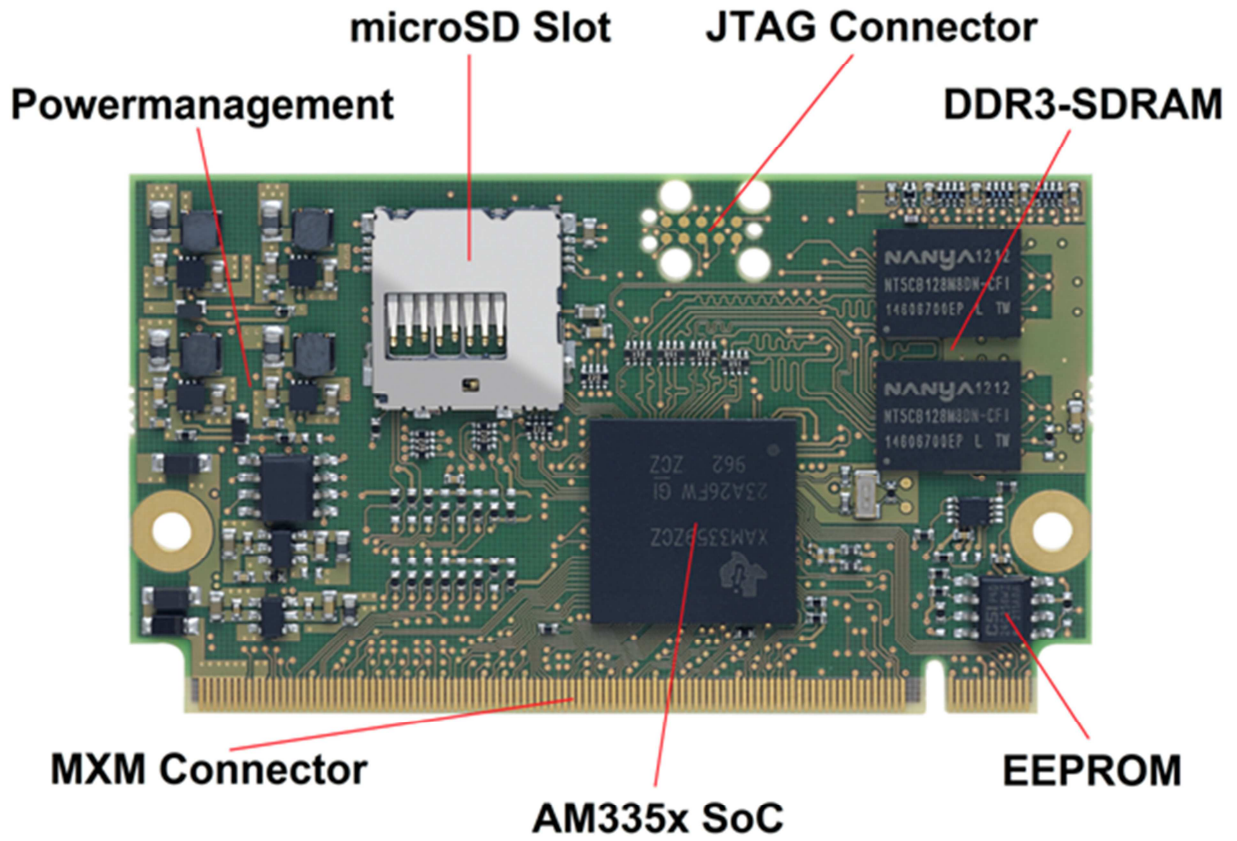


Figure 2: Overview Top

Component Placement

Top View

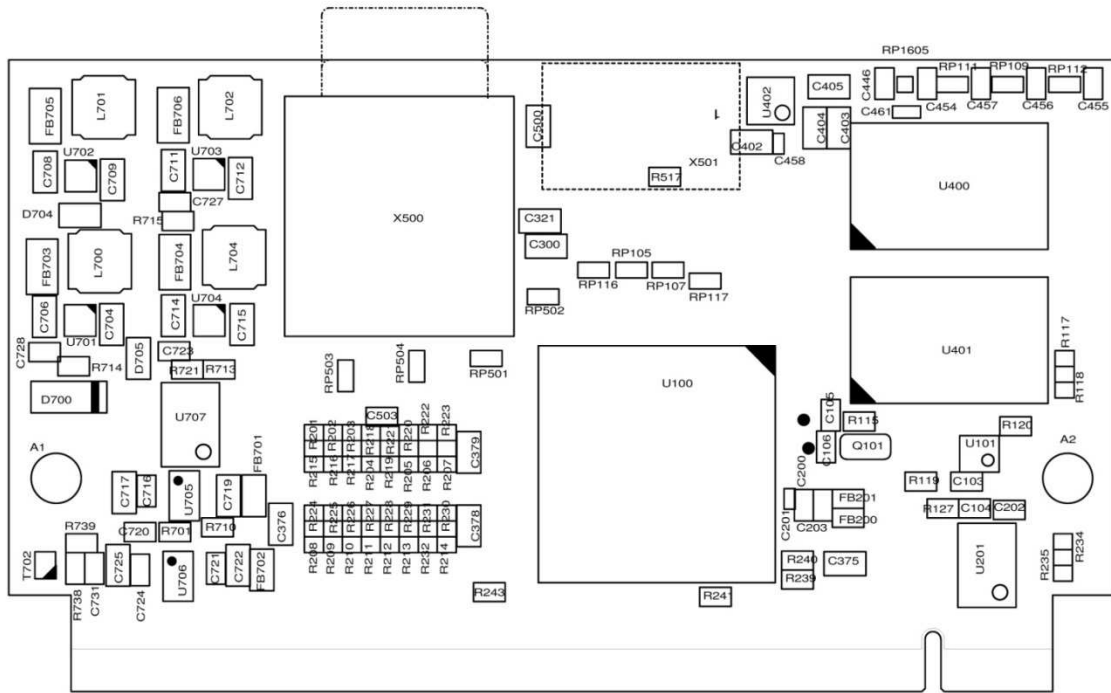


Figure 3: Component Placement - Top View

Bottom View

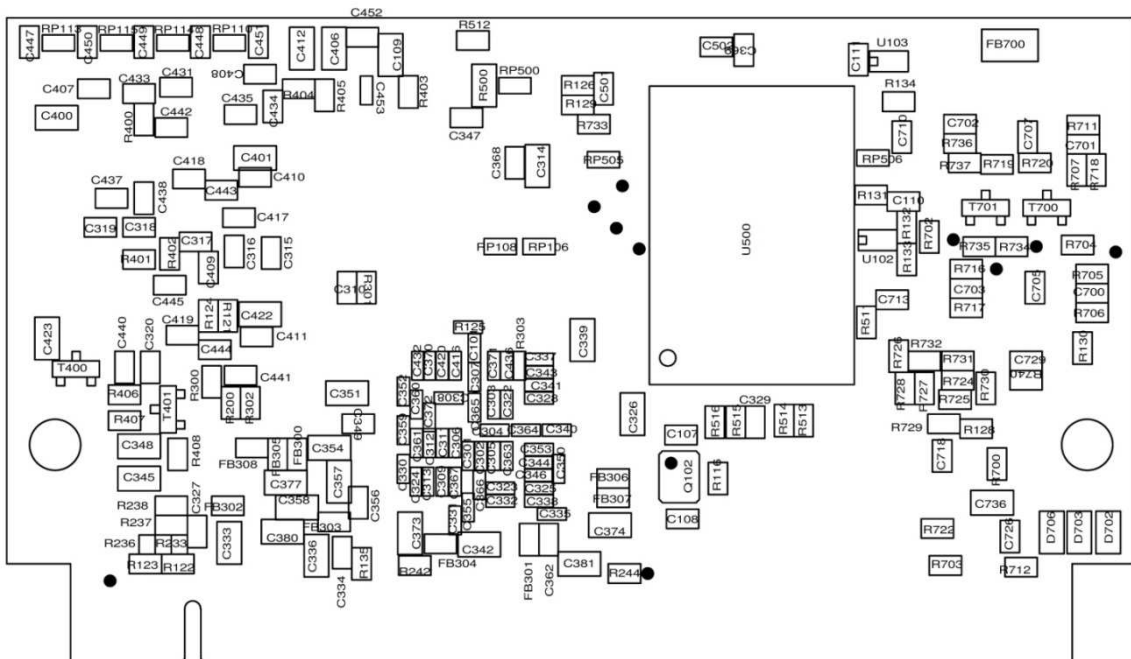


Figure 4: Component Placement - Bottom View

Power Supply

Primary System Power

The EPC35 operates off of a primary voltage supply with a nominal value of +5.0 V \pm 5%. On-board switching regulators generate the 1.1 V, 1.5 V, 1.8 V and 3.3 V voltage supplies required by the AM335x processor and on-board components from the primary 5.0 V supplied to the SOM.

For proper operation the EPC35 must be supplied with a voltage source of 5.0 V with at least 1.0 A capacity at the VCC pins on the EPC35 - Connector.

AM335x SoC

Description CPU

The AM335x microprocessors, based on the ARM Cortex-A8, are enhanced with image, graphics processing, peripherals and industrial interface options such as EtherCAT and PROFIBUS.

The AM335x microprocessor contains these subsystems:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8 microprocessor.
- POWERVR SGX Graphics Accelerator subsystem for 3D graphics acceleration to support display and gaming effects.
- The Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS) is separate from the ARM core, allowing independent operation and clocking for greater efficiency and flexibility. The PRU-ICSS enables additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos, and others [1].

Features

- Up to 1-GHz Sitara ARM Cortex-A8 32-Bit RISC Processor
 - NEON SIMD Coprocessor
 - 32KB of L1 Instruction and 32KB of Data Cache with Single-Error Detection (Parity)
 - 256KB of L2 Cache with Error Correcting Code (ECC)
 - 176KB of On-Chip Boot ROM
 - 64KB of Dedicated RAM
 - Emulation and Debug – JTAG
 - Interrupt Controller (up to 128 Interrupt Requests)
- 64KB of General-Purpose On-Chip Memory Controller (OCMC) RAM
- External Memory Interfaces (EMIF) DDR3 with 400-MHz Clock (800-MHz Data Rate)
- General-Purpose Memory Controller (GPMC)
 - Flexible 8-Bit Asynchronous Memory Interface with CS for NAND flash
 - Uses BCH Code to Support 4-, 8-, or 16-Bit ECC
 - Uses Hamming Code to Support 1-Bit ECC
- Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)
 - Supports Protocols such as EtherCAT, PROFIBUS, PROFINET, EtherNet/IP™
 - Two Programmable Real-Time Units (PRUs)
- Power, Reset, and Clock Management (PRCM) Module
- Real-Time Clock (RTC)
- Peripherals
 - Up to Two USB 2.0 High-Speed OTG Ports with Integrated PHY
 - Up to Two Industrial Gigabit Ethernet MACs (10, 100, 1000 Mbps)
 - Up to Two Controller-Area Network (CAN) 2.0 A/B
 - Up to Two Multichannel Audio Serial Ports (McASPs)
 - Up to Six UARTs with IrDA and CIR Modes Support
 - Up to Two Master and Slave McSPI Serial Interfaces
 - Up to Three MMC, SD, SDIO Ports
 - Up to Three I²C Master and Slave Interfaces
 - Up to Four Banks of General-Purpose I/O (GPIO) Pins
 - Up to Three External DMA Event Inputs (Interrupt Inputs)
 - Eight 32-Bit General-Purpose Timers
 - One Watchdog Timer
 - SGX530 3D Graphics Engine
 - Advanced Shader Feature Set in Excess of Microsoft VS3.0, PS3.0, and OGL2.0
 - Industry Standard API Support of Direct3D Mobile, OGL-ES 1.1 and 2.0, OpenVG 1.0, and OpenMax
 - LCD Controller
 - Up to 24-Bit Data Output; 8 Bits per Pixel (RGB)
 - Resolution up to 2048 x 2048 (with Maximum 126-MHz Pixel Clock)
 - Integrated LCD Interface Display Driver Controller and Raster Controller
 - 12-Bit Successive Approximation Register (SAR) ADC
 - Can be Configured to Operate as a 4-wire, 5-wire, or 8-wire Resistive Touch Screen Controller (TSC) Interface
 - Up to Three 32-Bit eCAP Modules
 - Up to Three Enhanced High-Resolution PWM Modules (eHRPWMs)
 - Up to Three 32-Bit Enhanced Quadrature Encoder Pulse (eQEP) Modules
 - Debug Interface Support
 - On-Chip Enhanced DMA Controller (EDMA)
 - Inter-Processor Communication (IPC) for Process Synchronization Between Cortex-A8, PRCM, and PRU-ICSS
 - Security: Crypto Hardware Accelerators (AES, SHA, PKA, RNG)
 - Package: 324-Pin S-PBGA-N324 Package (ZCZ Suffix), 0.80-mm Ball Pitch
 - Available in commercial, industrial and extended temperature range [2]

Parameters

AM335x SoC	
ARM CPU	1x ARM Cortex-A8
ARM MHz (Max.)	Up to 1000
ARM MIPS (Max.)	Up to 2000
Graphics Acceleration	1x 3D POWERVR® SGX530 core
Other Hardware Acceleration	2 PRU-ICSS, Crypto Accelerator
On-Chip L1 Cache	64 KB (ARM Cortex-A8)
On-Chip L2 Cache	256 KB (ARM Cortex-A8)
Other On-Chip Memory	128 KB
Display Options	24 bit LCD
General Purpose Memory	8-bit (GPMC, NAND)
DRAM	16-bit (DDR3-800)
USB	Up to 2
EMAC	2-Port Switch 10/100/1000
MMC/SD	Up to 3
CAN	Up to 2
EtherCAT Slave	AM3359 only
UART	Up to 6
ADC	8-ch 12-bit
PWM (Ch)	Up to 3
eCAP	Up to 3
eQEP	Up to 3
RTC	Yes
I2C	Up to 3
McASP	Up to 2
SPI	Up to 2
DMA (Ch)	64-Ch EDMA
IO Supply (V)	3.3
Operating Temperature Range (°C)	Commercial 0 to 90
Operating Temperature Range (°C)	Industrial -40 to 90
Operating Temperature Range (°C)	Extended -40 to 105

Table 2: AM335x Parameters [3]

Functional Block Diagram

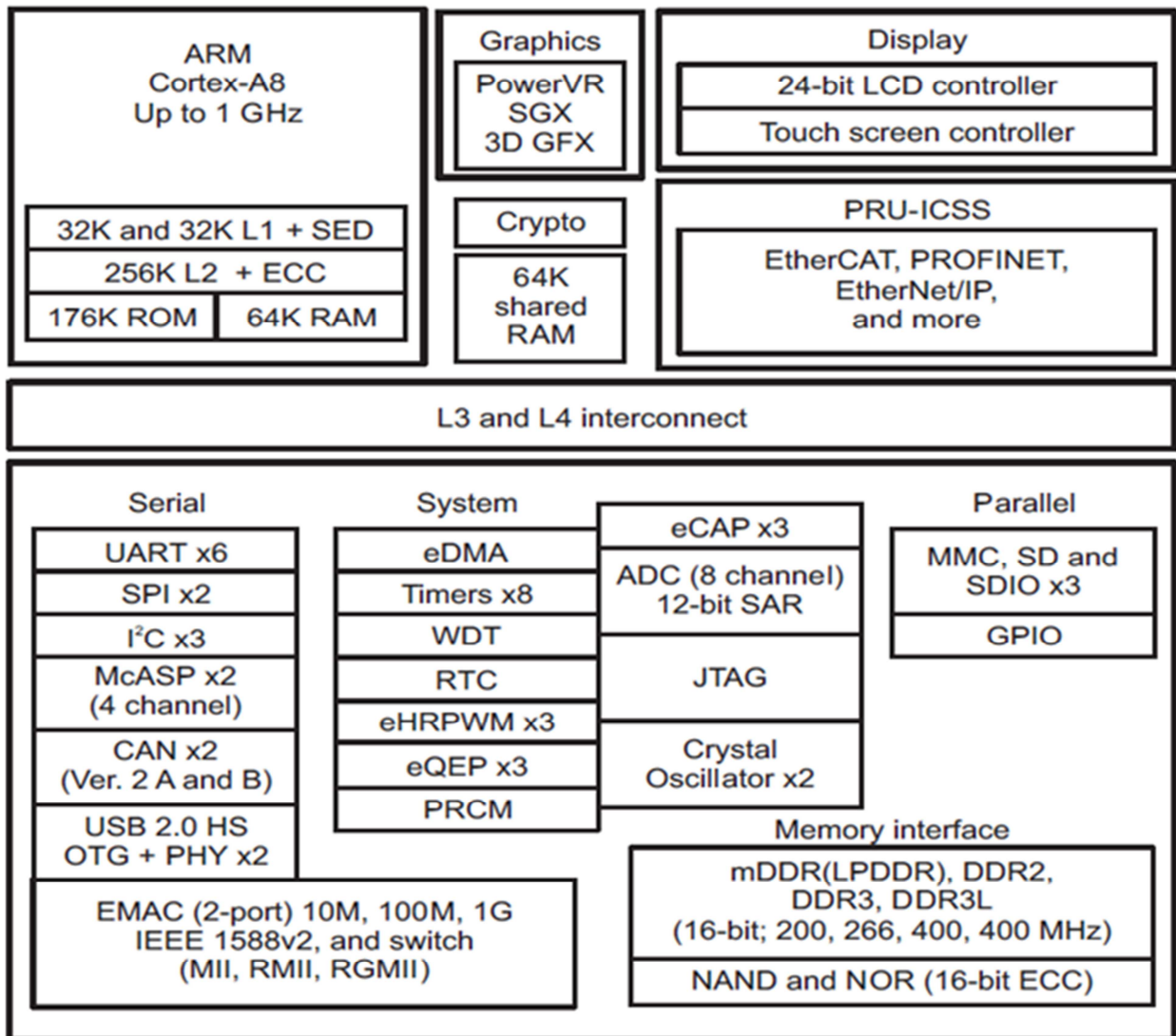


Figure 5: AM335x Block Diagram [4]

PRU

The Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS) is separate from the ARM core, allowing independent operation and clocking for greater efficiency and flexibility. The PRU-ICSS enables additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos.

DDR3-SDRAM

The RAM memory of the EPC35 is comprised of two 8-bit wide DDR3-SDRAM chips. The effective bus is 16-bits wide.

The DDR3-SDRAM memory is accessed via the EMIF0 port starting at 0x8000 0000. Typically the DDR3-SDRAM initialization is performed by a boot loader.

Power-on reset and must not be changed at a later point by any application code. Refer to the AM335x Technical Reference Manual about accessing and configuring these registers.

NAND-Flash

NAND Flash 8 bit width asynchronous or synchronous memory or device
8 bit: non burst device only, up to 64GB, up to 16Bit EEC.

EEPROM

The CAT24C256 is a 256 kb Serial CMOS EEPROM, internally organized as 32,768 words of 8 bits each.

It features a 64byte page write buffer and supports the Standard 100 kHz), Fast 400 kHz and Fast-Plus 1 MHz I2C protocol.

On-Chip ECC (Error Correction Code) makes the device suitable for high reliability applications

Mechanical Dimension

Drawing

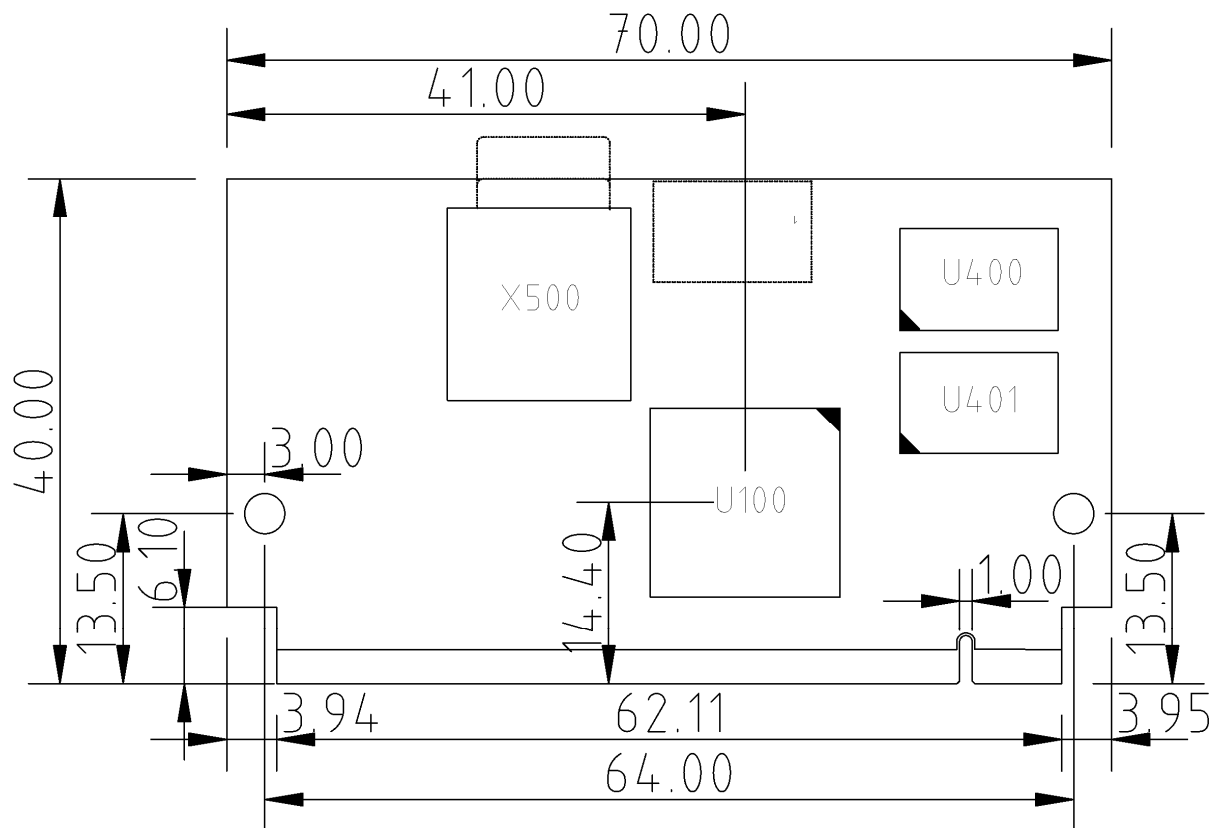


Figure 6: Mechanical Dimension - Drawing

Dimension/Weight

Dimensions	40 mm x 70 mm
Board	1,2 mm
Component height top	2 mm
Component height bottom	2 mm
Weigth	~ 20 g

Table 3: Mechanical Dimension - Dimension/Weight

Boot Configuration

Placement of boot device selection resistors

The boot device selection resistors are placed pad on pad to avoid wrong configurations.

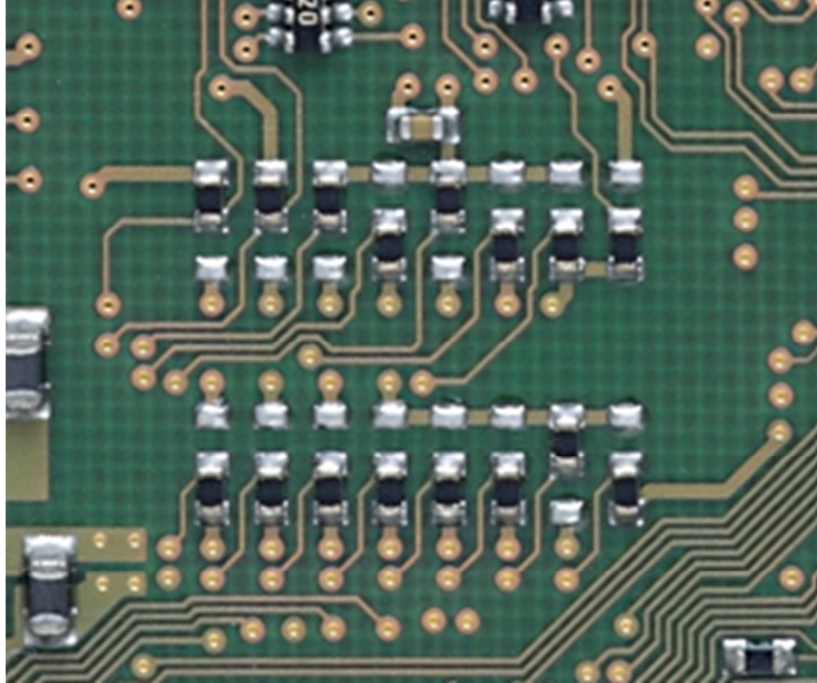


Figure 7: Boot selection resistors

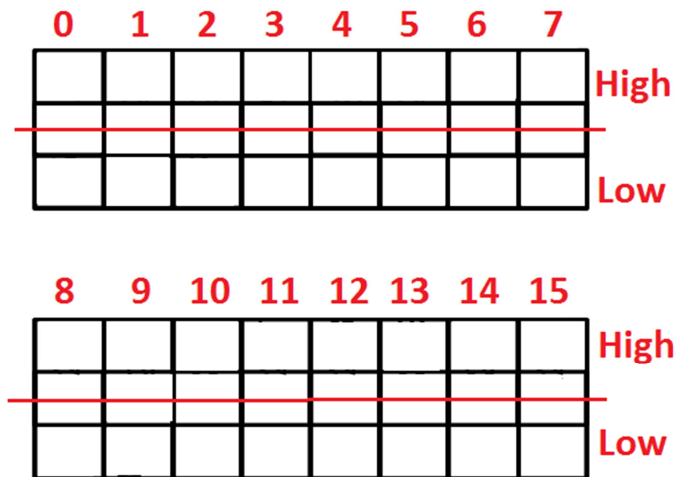


Figure 8: Placement of boot selection resistors

Placement of boot device selection resistors

The boot modes can be changed via the configuration SYSBOOT[4:0]. Please refer to chapter 26.1.5.2.1 SYSBOOT Configuration Pins Table 26-7 from Datasheet. [4]
The default configuration is 10011b.

Interface

Module plug connectors

MXM Connector
0,5 mm Pitch, 230 pol.



Figure 9: MXM Connector

Manufacturer	Order number
Foxconn	ASOB32*-S78Q-7H
YAMAICHI	BEC-0.5-230-S9-BFR-EDC
Aces Electronic Co., Ltd.	88882-2D0*

Table 4: List of manufacturers

Connector - Pin assignment and signal description

Pin	PIN-NAME	PULLUP/ PULLDOWN _VALUE	Pin	PIN-NAME	PULLUP/ PULLDOWN _VALUE	Pin	PIN-NAME	PULLUP/ PULLDOWN _VALUE	
1	GND		39	GND		77	N.C.		
2			40			78			
3	AIN0		41	N.C.		79			
4	AIN1		42		80				
5	AIN2		43		81				
6	AIN3		44		82				
7	AIN4		45		83	UART1_RXD			
8	AIN5		46		84	UART1_TXD			
9	AIN6		47		85	UART1_RTSn			
10	AIN7		48		86	UART1_CTSn			
11	EMU0	PU_100k	49		87	UART0_RXD			
12	EMU1		50		88	UART0_TXD			
13	EXTINTn	PD_100k	51		89	UART0_RTSn			
14	POK_1.8V_RTC*		52		90	UART0_CTSn			
15	EXT_WAKEUP	PU_10k	53		91	N.C.			
16	WARMRSTn	PU_10k	54		92				
17	WARMRSTn	PU_10k	55	93					
18	PMIC_POWER_EN		56	94					
19	N.C.		57	GND		95	GND		
20			58			96			
21			59	ECAP0_IN_PWM0_OUT	97				
22			60	N.C.	98				
23	GND		61	N.C.		99	MMC0_DAT3	PU_10k	
24			62	N.C.	100	MMC0_DAT2	PU_10k		
25			63	N.C.	101	MMC0_DAT1	PU_10k		
26	XDMA_EVENT_INTR0		64	SPI0_CS1 used as MMC_CD	PU_10k	102	MMC0_DAT0	PU_10k	
27	MCASP0_ACLKX		65	SPI0_CS0		103	MMC_CLK	PU_10k	
28	MCASP0_AHCLKX		66	SPI0_D1		104	MMC_CMD	PU_10k	
29	MCASP0_ACLKR		67	SPI0_D0		105	RMII1_REF_CLK		
30	MCASP0_FSX		68	SPI0_SCLK		106	MII1_COL		
31	MCASP0_AHCLKR		69	N.C.		107	MII1_CRS		
32	MCASP0_FSR		70			108	MII1_RX_ER		
33	MCASP0_AXR0		71	I2C0_SDA	PU_4.7k	109	MII1_TX_EN		
34	GND		72	I2C0_SCL	PU_4.7k	110	MII1_TXD3		
35	XDMA_EVENT_INTR1		73	GND		111	MII1_TXD2		
36	N.C.		74			112	MII1_TXD1		
37	MCASP0_AXR1		75	N.C.		113	MII1_TXD0		
38	N.C.		76			114	MII1_TX_CLK		

Pin	PIN-NAME	PULLUP/ PULLDOWN _VALUE	Pin	PIN-NAME	PULLUP/ PULLDOWN _VALUE	Pin	PIN-NAME	PULLUP/ PULLDOWN _VALUE
115	MII1_RX_DV		154	GPMC_A7		193	LCD_DATA0	
116	MII1_RXD3		155	N.C.		194	LCD_DATA1	
117	GND		156	GPMC_WPh	PU_10k	195	LCD_DATA2	
118			157	GPMC_BEn1		196	LCD_DATA3	
119	MII1_RXD2		158	GPMC_ADVn_ALE		197	GND	
120	MII1_RXD1		159	GND		198		
121	MII1_RXD0		160	GND		199	LCD_DATA4	
122	MII1_RX_CLK		161	GPMC_OEn_Ren		200	LCD_DATA5	
123	MDIO		162	GPMC_WEn		201	LCD_DATA6	
124	MDC		163	GPMC_BEn0_CLE		202	LCD_DATA7	
125	USB0_DRVVBUS		164	GPMC_AD0		203	LCD_DATA8	
126	USB1_DRVVBUS		165	GND		204	LCD_DATA9	
127	USB0_CE		166			205	LCD_DATA10	
128	USB1_CE		167	GPMC_AD1		206	LCD_DATA11	
129	USB0_ID		168	GPMC_AD2		207	LCD_DATA12	
130	USB1_ID		169	GPMC_AD3		208	LCD_DATA13	
131	USB0_DM		170	GPMC_AD4		209	LCD_DATA14	
132	USB1_DM		171	GPMC_AD5		210	LCD_DATA15	
133	USB0_DP		172	GPMC_AD6		211	GND	
134	USB1_DP		173	GPMC_AD7		212		
135	GND		174	GPMC_CSn0	PU_10k	213		
136			175	GPMC_CSn1		214		
137	USB0_VBUS		176	GPMC_CSn2		215	POK_VDD*	PU_10k
138	USB1_VBUS		177	GPMC_CSn3		216	FWR_FAIL_IN*	
139	GPMC_A0		178	GPMC_CLK		217	VCC	
140	GPMC_A2		179	GPMC_AD8		218		
141	GND		180	GPMC_AD9		219		
142			181	GPMC_AD10		220		
143	GPMC_A3		182	GPMC_AD11		221		
144	GPMC_A4		183	GND		222		
145	GPMC_A5		184			223		
146	GPMC_A6		185	GPMC_AD12		224		
147	GND		186	GPMC_AD13		225		
148			187	GPMC_AD14		226		
149	GPMC_A1		188	GPMC_AD15		227		
150	GPMC_A8		189	LCD_VSYNC		228		
151	GPMC_A9		190	LCD_HSYNC		229		
152	GPMC_A10		191	LCD_PCLK		230		
153	GPMC_A11		192	LCD_AC_BIAS_EN				

Table 5: Connector - Pin assignment and signal description

Description of signals *)

Name	Description
VCC	5.0 V DC ± 5% system power
GND	0 V Ground
POK_1.8V_RTC*	Power Good output from 1.8V RTC LDO [1.8V logic]
POK_VDD*	Power Good output from Core and MPU switching regulators[1.8V logic]
FWR_FAIL_IN*	RESERVED

Table 6: Description of Signals

Used Signals for IIC EEPROM, NAND Flash, micro SD

Used Signals for IIC EEPROM

Pin	PIN-NAME	Description
71	I2C0_SDA	Data
72	I2C0_SCL	Clock

Table 7: Used Signals for IIC EEPROM

Used Signals for NAND Flash

Pin	PIN-NAME	Description
156	GPMC_WPn	Write Protect [low active]
158	GPMC_ADVn_ALE	Address latch enable [high active]
161	GPMC_OEn_Ren	Read enable [low active]
162	GPMC_WEn	Write enable [low active]
163	GPMC_BEn0_CLE	Command latch enable [high active]
164	GPMC_AD0	I/O1
167	GPMC_AD1	I/O2
168	GPMC_AD2	I/O3
169	GPMC_AD3	I/O4
170	GPMC_AD4	I/O5
171	GPMC_AD5	I/O6
172	GPMC_AD6	I/O7
173	GPMC_AD7	I/O8
174	GPMC_CSn0	Chip enable [low active]
-	GPMC_WAIT0	Ready/Busy [low active]

Table 8: Used Signals for NAND Flash

Used Signals for micro SD Card

Pin	PIN-NAME	Description
64	SPI0_CS1 used as MMC_CD	Card Detect
99	MMC0_DAT3	I/O4
100	MMC0_DAT2	I/O3
101	MMC0_DAT1	I/O2
102	MMC0_DAT0	I/O1
103	MMC_CLK	Clock
104	MMC_CMD	Command

Table 9: Used Signals for micro SD Card

Product Features and Specifications

Product Key – Ordering Information

See Price and Ordering Information (POI) sheet.

Function Description: Interfaces

micro SD

Standard micro can be used. SD Card interface complies with MMC4.3 and SD and SDIO 2.0 Specifications. Contacts are on top side.

JTAG

JTAG (Joint Test Action Group) is the common name for IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture.

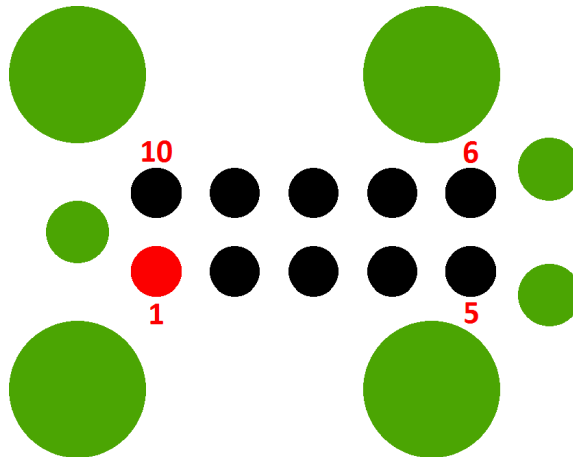


Figure 10: JTAG Connector

JTAG	Direction	Signal	PULLUP/ PULLDOWN _VALUE
1	O	nRESET	PU_10k
2	O	JTAG_TDI	PU_10k
3	I	JTAG_TDO	PU_10k
4	O	JTAG_TMS	PU_10k
5	O	JTAG_TCK	PD_10k
6	O	nRESET	PU_10k
7		DGND	
8		DGND	
9		DGND	
10		+3.3V	

Table 10: JTAG Connector

Manufacturer	Order number
Tag-Connect	TC2050-IDC

Table 11: Tag-Connect

List of References

- [1] Texas Instruments Incorporated, "AM335x Processors - Description," [Online]. Available: <http://www.ti.com/product/am3359#descriptions>. [Accessed 25 11 2014].
- [2] Texas Instruments Incorporated, "AM335x Processors-Features," [Online]. Available: <http://www.ti.com/product/am3359#features>. [Accessed 25 11 2014].
- [3] Texas Instruments Incorporated, "AM335x Processors - Parametrics," [Online]. Available: <http://www.ti.com/product/am3359#parametrics>. [Accessed 25 11 2014].
- [4] Texas Instruments Incorporated, "AM335x Sitara™ Processors (Rev. G)," [Online]. Available: <http://www.ti.com/lit/ds/symlink/am3359.pdf>. [Accessed 25 11 2014].